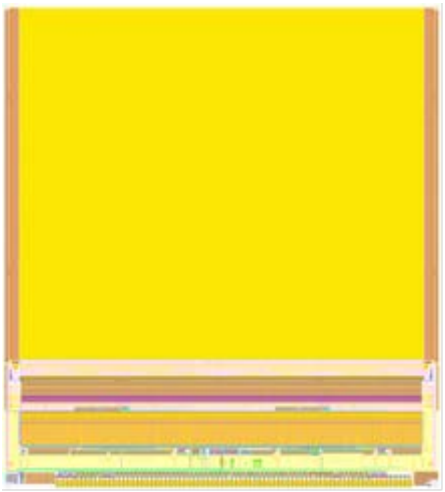
CAPELLA – CIS120
Back illuminated digital output
CMOS image sensor



Layout plot

FEATURES

- 2048 × 2048 pixels in a 20.48 mm square image area

  Pixel size is 10 µm square

- On-chip ADC, programmable from 8 to 14 bits

  Four LVDS data outputs at 260 Mbps

- Back-illuminated sensitivity and spectral response

  Excellent image quality

- Both rolling shutter (RS) and global shutter (GS) modes are available from the 5T pixels

  On-chip CDS or external DDS for low readout noise

- Configuration programmable by SPI

  Pin count minimised by on-chip timing control

- Good latch-up immunity and high SEU threshold by design

  Resistant to ionising radiation by process choice

OVERVIEW

CIS120 has been designed as an easy to use general purpose imager for space applications. Back-illumination, combined with low readout noise and on-chip analogue-to-digital conversion give excellent image quality.

Pixel read timing is set by an on-chip sequencer to simplify use and to reduce pin count.

A column parallel ADC is used to quantise each row of pixels in turn and is controlled by its own sequencer. Resolution can be set from 8 to 14 bits.

Four LVDS channels output the image data and are controlled by the readout sequencer to scan along each row in turn. Two LVDS synchronisation channels allow accurate data sampling.

All configuration settings are programmed over an SPI. This includes shutter mode, ADC resolution and bias current values.

Package options will range from a ceramic PGA to metal and ceramic three-side buttable designs for use in mosaic focal planes.

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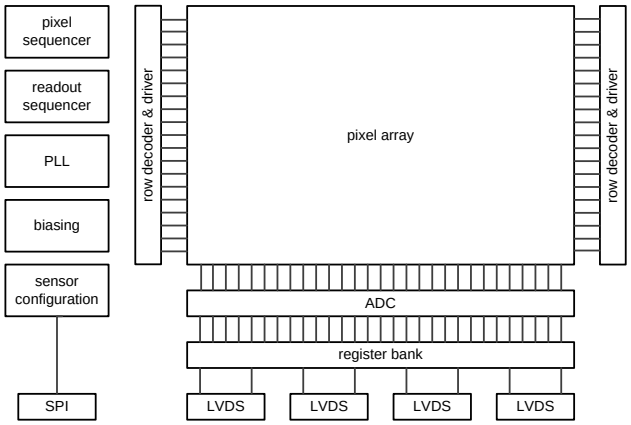
ARCHITECTURE



Architecture of CIS120.

The sensor configuration registers control all imager settings (including shutter mode, ADC resolution and bias values) and are programmed through an SPI interface. The pixel access is per row and driven by an on-chip pixel sequencer with separate row decoders for left and right halves of the pixel array.

The analogue pixel outputs are converted to digital values by a column parallel ADC with programmable resolution (8 to 14 bit). The digital words are stored in a register bank until serialised and output through the four LVDS data interfaces, with two LVDS for synchronisation. Readout timing is controlled by the on-chip readout sequencer. Frame rate is determined by ADC resolution, shutter mode and the use of ROI.

A programmable PLL can be used to generate the 130 MHz clocks for the ADC and the data output, from a range of external reference frequencies.

An on-chip programmable biasing block generates all required analogue bias currents from only four input reference currents and so helps to minimise the number of pins.

PACKAGES

All bond pads are located on one side of the chip to allow the use of a three-side buttable package, so larger focal plane arrays can be assembled. Early devices will be packaged in an existing ceramic PGA.

HIGH ENERGY RADIATION

CIS120 has been developed for use in space. By design the sensor is immune to latch-up and Single Event Upset (SEU) from charged particles up to 67 MeV·cm²/mg LET.

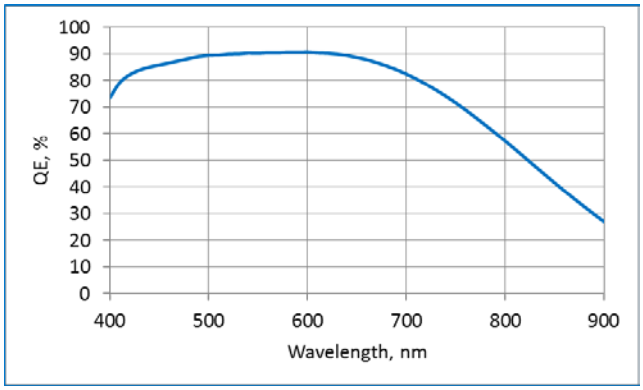
Performance parameters will begin to change if the device is subject to ionising radiation. Contact Teledyne e2v for further information.

TYPICAL PERFORMANCE

Number of pixels	2048 × 2048
Pixel size	10 µm × 10 µm
Image area	20.48 × 20.48 mm
Linear charge capacity	35 ke⁻/pixel
Conversion gain	40 µV/e⁻
Quantum efficiency @ 550 nm (BI)	90 %
Dark current at 20 °C	50 e⁻/pixel/s
Readout noise	4 e⁻ rolling shutter 11 e⁻ global shutter
ADC resolution	8, 10, 12 or 14 bit
Frame rate (rolling shutter and full frame)	30 fps @ 8bit, 20 fps @ 12bit
Outputs, LVDS or sub-LVDS	4 data + 2 sync
Output data rate	260 Mbps/channel
Setup and control bus	SPI
Clocks	4 MHz and 130 MHz
Power supplies	3.3V and 1.8V
Power consumption	<280 mW (sub-LVDS) <350 mW (LVDS)
Die size (width × height)	22.20 × 28.35 mm

SPECTRAL RESPONSE

A typical back illuminated spectral response (QE) with the ‘Multilayer-2’ AR coating is shown below:



VARIANTS

Devices with alternative AR coatings and spectral responses are possible as custom variants.

CIS120 is stitched, so other sizes are possible from 2048 × 1024 up to 2048 × 8192 pixels, without the cost of new masks.

An increased charge capacity of 100 ke⁻ is possible by a metal pattern change.

Contact Teledyne e2v for further information on these options.